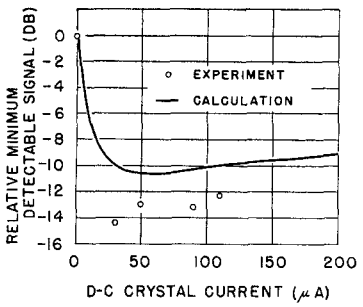

Fig. 5—Minimum detectable signal of 1N53 detector relative to zero bias.

the MDS at zero dc bias is S_0,

$$S_0 = F_0 N_i \tag{36}$$

where F_0 is the noise figure of the diode when no dc bias is applied. Thus the relative MDS S(db) can be expressed by

$$S(\text{db}) \equiv 10 \log \frac{S}{S_0} = 10 \log \frac{F}{F_0}$$
$$= F(\text{db}) = P(\text{db}) - G(\text{db}). \tag{37}$$

In Fig. 5 the calculated relative MDS and experimentally obtained relative MDS are plotted with zero bias MDS as zero db. The zero dc bias MDS of a 1N53 diode in a DBB119 crystal mount followed by a 441B amplifier was −50.8 dbm at 73.22 kMc. Experiment and calculation show that the MDS of the diode decreases with increasing dc bias current up to approximately 70 μa.

Conclusions

The conclusions which have been reached by theoretical analysis and experimental investigation are as follows:

1) Biasing the detector increases the noise generated in the crystal;
2) This increase in noise is small when compared with the increase in gain;
3) Thus, even though noise increases, the noise figure of a device can decrease.

Acknowledgment

Much of the numerical computation involved in this paper was performed at the Marquette University Computing Center. The authors thank the staff for their cooperation. The authors also thank Raytheon Company for contributing the klystron tubes as the signal source; and S. Krupnik, J. A. Stefancin, and J. E. Billo for their assistance.

Microwave Variable Attenuators and Modulators Using *PIN* Diodes*

J. K. HUNTON†, SENIOR MEMBER, IRE, AND A. G. RYALS†

Summary—The *PIN* diode is a double diffused junction with an intrinsic layer separating the *P* and *N* regions. At frequencies above 100 Mc, the diode ceases to be a rectifier because of carrier storage and transit time effects. Its shunt capacitance is quite small because of the separation of the *P* and *N* regions by the *I* layer. Conductivity of the *I* region can be varied by a dc bias current and the device becomes an electrically variable resistor which can be used for microwave attenuators and modulators up to frequencies as high as 20 Gc.

The *PIN* junctions are mounted on posts which are inserted in a 50-ohm strip transmission line as shunt elements, and a number of these elements, spaced a quarter wavelength apart at midband, are used to form an attenuator. At the appropriate bias current, yielding 50-ohm junction resistances, the diode elements are reactively compensated by choice of post dimensions so that they are effectively pure resistances, yielding an image attenuation of 4.2 db per element. Many elements can be used to attain any desired total attenuation and higher impedance end elements can be used to improve the SWR. Bandwidths of 4 to 1 with low SWR in both ON and OFF conditions are achievable. Maximum attenuation of 60 db, insertion loss of 1 db, and SWR of 1.5 are typical for a 12-diode attenuator and powers of the order of watts can be handled with negligible harmonic generation. When used as a pulse modulator, rise times of the order of 10 nsec are achievable.

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I. Introduction

THE POTENTIAL application of a *PIN* junction diode as an electrically variable resistance element at microwave frequencies was discussed by Uhlir in an earlier paper.[1] It is the purpose of this paper to show how these junctions can be combined with appropriate broad-band microwave networks to produce electrically controllable attenuators and pulse modulators. The goal is an attenuator which is capable of a large attenuation range with low insertion loss and low SWR and which can be used as a leveling device, programmable attenuator, or pulse modulator in frequency ranges from 1 to 20 kMc.

An attenuating array is composed of metal posts, on which are cemented tiny *PIN* junctions, inserted as shunt elements in a transmission line and spaced a quarter wavelength apart at the middle of the frequency band involved. By suitable post design, reactive compensation is achieved and the diode elements appear as an array of shunt resistances when biased with the appropriate current. When at zero bias, the elements form an array of shunt capacitances. In both cases the attenuator can be analyzed by image parameter methods. Good agreement exists between experimental and theoretical results and broad-band attenuators are realized which satisfy the original goals.

Much work has been done on semiconductor switching devices[2] which achieve very fast rise times of the order of 1 nsec. These devices have employed fast diodes of the point-contact germanium or *P-N* junction varactor-type, usually as single elements, behaving somewhat as switchable reactive filters. Although they are faster than the *PIN* attenuators to be described here, they appear to be unsuitable for continuous control of attenuation with low SWR and low harmonic generation. It is also difficult with these devices to achieve as broad a bandwidth at the higher frequencies or as high an ON-OFF ratio with low insertion loss when compared with the *PIN* attenuating array.

The *PIN* diode is a double diffused silicon junction with an intrinsic layer separating the *P* and *N* regions. At very low frequencies it behaves as a normal rectifier. Forward conduction increases exponentially with applied voltage as the *I* (intrinsic) layer conductivity is increased by the presence of injected carriers. At high frequencies, above 100 Mc, rectification effectively ceases because of carrier storage effects and transit time. The junction becomes a linear resistance with the conductivity of the *I* layer and its geometry being the determining factors in the resistance value. This conductivity is a function of the carrier density which can be controlled by a bias current. Approximately, the diode resistance is proportional to the square of the *I* layer thickness and inversely proportional to the product of bias current and carrier lifetime. Of course there is capacitance shunting the resistance. However, this capacitance is very small because of the relatively thick *I* layer separating the *P* and *N* regions and the small area of the junction. Typical diodes can be varied in resistance from 10,000 ohms to 10 ohms as bias current is varied from zero to several milliamperes and the shunt capacitance at zero bias is typically of the order of 0.04 pf.

II. Diode Mounting Structures and Equivalent Circuit

The *PIN* junctions are mounted on posts which are to be inserted as shunt elements in a strip transmission line. Fig. 1 shows a cross-section view of a 50-ohm unsymmetrical strip-line and mounting structure along with the Smith Chart admittance plot obtained at 4000 Mc by varying the bias current from zero to 15 ma. The data was obtained by measuring the reflection coefficient of the diode element in parallel with a 50-ohm load. This load admittance was then subtracted from the total admittance measured to obtain the actual diode element admittance plotted on the chart.

A simple way of looking at the diode mounting structure is to consider it as an elemental transmission line terminated in the parallel resistance and capacitance of the diode junction and connected in shunt with the main transmission line. If the junction capacitance is negligible and if the elemental line or post has an impedance equal to that of the main line (Z_0), the reflection coefficient as plotted on the Smith Chart would be simply

$$\Gamma = \frac{R/Z_0 - 1}{R/Z_0 + 1} e^{-2j(\omega l_p/v_p)},$$

where R is the resistance of the diode junction, a function of bias current, l_p is the post length, and v_p the phase velocity on the elemental line. Notice that, at any given frequency, the Smith Chart plot would be a straight line through the origin as R is varied from zero to infinity, intersecting the origin at $R=Z_0$ and, as frequency is varied, the plot simply rotates. At the appropriate bias current the diode element would be a pure resistance at all frequencies. At zero bias, the element would be a shunt capacitance with normalized susceptance $j(\omega l_p/v_p)$. This capacitance can be small provided the electrical length of the post is appropriately small. Although this picture of the diode element is oversimplified, it provides the basis for the design of broad-band attenuating elements.

As shown in Fig. 1, the diode mounting post within the main line is a series of steps which approximate a

[1] A. Uhlir, Jr., "The potential of semiconductor diodes in high-frequency communications," Proc. IRE, vol. 46, pp. 1099–1115; June, 1958.

[2] R. V. Garver, "Theory of TEM diode switching," IRE Trans. on Microwave Theory and Techniques, vol. MTT-9, pp. 224–238; May, 1961.

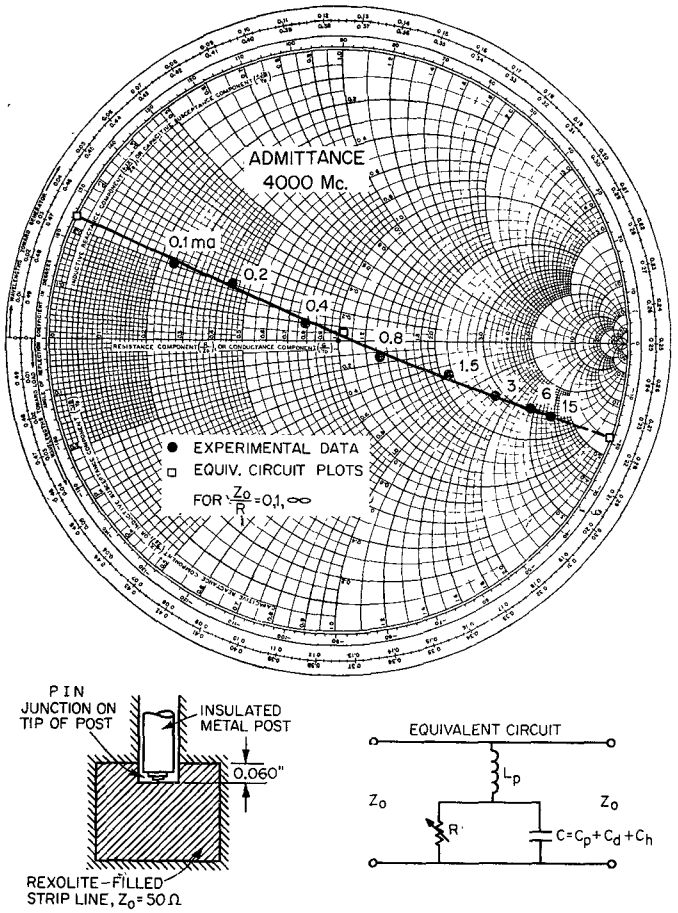


Fig. 1—Diode element mounting structure in unsymmetrical strip-line, equivalent circuit representation, and experimental Smith Chart admittance plot as a function of bias current at 4000 Mc.

TABLE I

EQUIVALENT CIRCUIT VALUES FOR FIG. 1

Post length, l_p	0.060 in
Post Inductance, L_p	0.33 nh
Circuit Capacitance, C	0.17 pf
Circuit Impedance, $Z_c=\sqrt{L_p/C}$	44 Ω
Cutoff Frequency, $f_0=1/(2\pi\sqrt{L_pC})$	21.2 Gc
Junction Capacitance, C_d	0.04 pf
Hole Capacitance, C_h	−0.05 pf
Post Capacitance, $C_p=C-C_d-C_h$	0.18 pf
Post Impedance, $Z_p=\sqrt{L_p/C_p}$	43 Ω
Post Phase Velocity, $v_p=l_p/\sqrt{L_pC_p}$	2.0×10^{10} cm/sec

short conical transmission line. The small *PIN* junction is cemented on the bottom of the post and contacts the center conductor strip. The post itself is coated with insulating material to form a bypass capacitance in the upper ground plane hole, and a dc return is provided elsewhere in the system. The main transmission line is unsymmetrical, in this model, with the center conductor strip much closer to the top than to the bottom ground plane. A hole is provided in the dielectric for insertion of the diode post.

If R in the above reflection coefficient equation is replaced by the impedance of the parallel junction resistance and capacitance combination, it is obvious that the Smith Chart plot is no longer a straight line. Deviation is greater at higher frequencies as the capacitive susceptance of the junction increases. It is much more convenient to represent the diode post and junction structure by an equivalent circuit of the form shown in Fig. 1 and to derive the element values from the experimental Smith Chart plot. Retaining a portion of the elemental transmission line idea, a circuit impedance $Z_c=\sqrt{L_l/C}$, and a cutoff frequency $\omega_0=1/\sqrt{L_pC}$ are defined. The post inductance is $L_p=Z_c/\omega_0$ and the capacitance, which includes the *PIN* junction capacitance as well as the post capacitance, is $C=1/\omega_0Z_c$. The equivalent circuit admittance is then,

$$\frac{Y}{Y_0}=\frac{Z_0}{Z}=\frac{Z_0/R+j(\omega/\omega_0)Z_0/Z_c}{1-\omega^2/\omega_0^2+j(\omega/\omega_0)(Z_c/Z_0)Z_0/R}.$$

At frequencies well below cutoff, this plots as a straight line and intersects the origin of the chart if $Z_c=Z_0$. The equivalent circuit values for Fig. 1 are derived from the experimental data and are listed in Table I. A further breakdown of the capacitance value is made on the basis of some further measurements. The hole in the dielectric of the strip-line, into which the diode is inserted, contributes a negative capacitance. By measuring the reflection coefficient of the dielectric hole, followed by a 50-ohm load, the negative capacitance was determined to be of the order of 0.05 pf. The zero-bias capacitance of the *PIN* junction itself was measured to be of the order of 0.04 pf, by a method described later. The remainder of the total circuit capacitance is then contributed by the post. A post impedance and phase velocity can be computed as shown in the table.

Fig. 2 shows a symmetrical strip-line cross section with two diodes, one from each side, in parallel. By a cut-and-try procedure the step dimensions on the posts were modified until the admittance plot, as shown in Fig. 2, passed very nearly through the origin of the Smith Chart. One diode was then removed and the corresponding dielectric hole plugged to obtain the admittance plot for the single diode shown also in Fig. 2. A very interesting effect occurs here. One might expect that the inductance in the equivalent circuit for the single post would be about double that of the two in parallel and the capacitance would be about one half. Reference to the equivalent circuit values listed in Table II and derived from the experimental Smith Chart plots does show the circuit capacitance for the single post case about one half that of the parallel case. But the inductance for the single case is about 8 times higher than the parallel case. This indicates that a mutual inductance coupling exists in the case of the

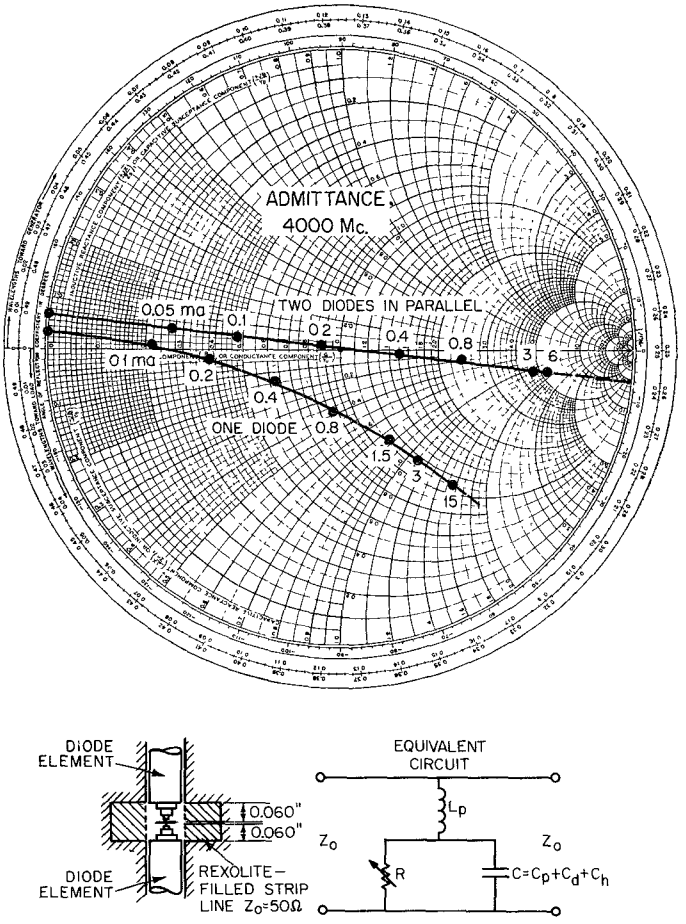


Fig. 2—Two diode elements mounted in parallel in symmetrical strip-line, equivalent circuit representation and experimental admittance plots as a function of bias current at 4000 Mc. One plot is for two diodes as shown in the cross-section view. The other plot is for the case of one diode removed and the corresponding dielectric hole plugged.

TABLE II

EQUIVALENT CIRCUIT VALUES FOR FIG. 2

	Single diode	Two diodes in parallel
Post Length, l_p	0.060 in	0.060 in each
Post Inductance, L_p	0 88 nh	0.106 nh
Circuit Capacitance, C	0.023 pf	0 051 pf
Circuit Impedance, $Z_c=\sqrt{L_p/C}$	195 Ω	45.5 Ω
Cutoff Frequency, $f_0=1/(2\pi\sqrt{L_pC})$	35.3 Gc	68.5 Gc
Junction Capacitance, C_d	0.04 pf	0 08 pf
Hole Capacitance, C_h	−0 05 pf	−0.1 pf
Post Capacitance, $C_p=C-C_d-C_h$	0.033 pf	0.071 pf
Post Impedance, $Z_p=\sqrt{L_p/C_p}$	163 Ω	39 Ω
Post Phase Velocity $v_p=l_p/\sqrt{L_pC_p}$	2.8×10^{10} cm/sec	

paralleled posts which reduces considerably the effective circuit inductance. The end result of combining two diodes in parallel is to increase the cutoff frequency by a factor of three when comparing Figs. 1 and 2. The structure shown in Fig. 1 was made unsymmetrical with the strip closer to the upper ground plane than to the lower, with the idea in mind that the single post inductance would be less than it would be if the structure were symmetrical. The improvement turned out to be only a minor one, however. With two diodes in parallel there is one disadvantage, namely, the reduction in zero-bias resistance by a factor of two. As will be shown later, this can result in a considerable increase in the insertion loss of attenuators made in this form.

A third structure investigated was a ridged waveguide, designed for a 50-ohm characteristic impedance. No dielectric was used and the gap, or effective post length, was made 0.030 inch which is just half the gap used for the strip-line structures. The post geometry, similar to that used in the structure of Fig. 1, is shown in the cross-section sketch in Fig. 3. Adjustments were made on the cut-and-try basis to make the Smith Chart admittance plots pass close to the origin. These experimental plots are shown in Fig. 3 for two frequencies with bias current as the variable. The derived equivalent circuit values are given in Table III and equivalent circuit plots are shown on the Smith Chart for $Z_0/R=0$, 1, and ∞, indicating good agreement of the circuit with experimental data. As might be expected, the cutoff frequency is approximately doubled by reducing the post length by a factor of two, comparing Figs. 1 and 3.

To obtain an approximate value of the junction capacitance C_d used in all the tables of equivalent circuit values, a measurement was made in the ridge waveguide structure of a post on which the *PIN* junction was replaced by a thin Mylar plastic sheet. Comparing the reflection coefficients measured for the two cases, and computing the capacitance at the post tip with the Mylar in place of the junction, the *PIN* junction capacitance value could be estimated. The value of $C_d=0.04$ pf is an average of several such measurements with different posts and *PIN* junctions. The range of values determined was from 0.035 to 0.045 pf.

Summarizing the results of equivalent circuit investigations, the highest cutoff frequency is obtained when the mounting post length is made as short as possible, the final limit being determined by the diode junction capacitance. The structure of Fig. 1 is suitable for attenuators up to a limiting frequency of 4 Gc, and the ridged waveguide structure of Fig. 3 is suitable in the *X*-band region up to 13 Gc. The dual diode structure of Fig. 2, although introducing added insertion loss, has the highest cutoff frequency, and could be used up to frequencies as high as 13 Gc, bearing in mind that the cross-section width must be reduced sufficiently to reject a waveguide-type propagation mode. In regard to the equivalent circuit representation, one might question the validity of the simple circuit where all capacitance is lumped in one place. More accurately, it should be divided in some manner on either side of the inductance. However, in the frequency ranges used, where

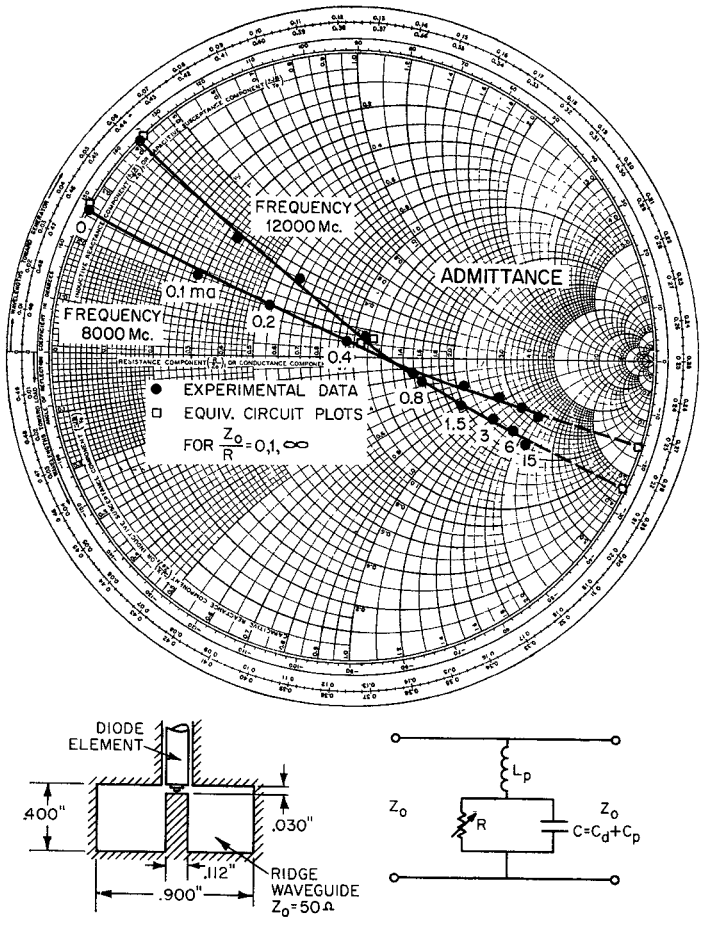


Fig. 3—Cross-section view of a diode element mounted in 50-ohm ridge waveguide, and experimental admittance plots as a function of bias current at 8 Gc and 12 Gc.

TABLE III
EQUIVALENT CIRCUIT VALUES FOR FIG. 3

Post Length, l_p	0.030 in
Post Inductance, L_p	0.148 nh
Circuit Capacitance, C	0.1 pf
Circuit Impedance $Z_c=\sqrt{L_p/C}$	38.4 Ω
Cutoff Frequency, $f_0=1/(2\pi\sqrt{L_pC})$	41.3 Gc
Junction Capacitance, C_d	0.04 pf
Post Capacitance, $C_p=C-C_d$	0.06 pf
Post Impedance, $Z_p=\sqrt{L_p/C_p}$	50 Ω
Post Phase Velocity, $v_p=l_p/\sqrt{L_pC_p}$	2.6×10^{10} cm/sec

operation is in the neighborhood of 0.25 ω_0 or less, very little difference in behavior occurs when using a more complicated equivalent circuit.

III. The Attenuating Array

As mentioned before, many diode elements spaced a quarter wavelength apart at midband are used to form the attenuator. When the applied bias current is sufficient to produce sizeable attenuation, the characteristics of the attenuating array can be described in terms of the image parameters, assuming identical elements. The following relations are derived in Appendix I.

$$\Gamma_i = -\cos\theta - 2\frac{Y_0}{Y} j\sin\theta + \left[-\sin^2\theta\left(1+4\frac{Y_0^2}{Y^2}\right)+2\frac{Y_0}{Y}j\sin 2\theta\right]^{1/2}$$

$$\frac{1}{T_i} = \cos\theta + \frac{Y}{2Y_0} j\sin\theta + \left[-\sin^2\theta\left(1+\frac{Y^2}{4Y_0^2}\right)+\frac{Y}{2Y_0}j\sin 2\theta\right]^{1/2}$$

where Γ_i is the reflection coefficient looking into an infinite array of diode elements, $1/T_i$ is the voltage ratio loss per diode element in an infinite array, θ is the radian angular spacing of the diode elements ($\theta=(2\pi/\lambda)x$), and Y/Y_0 is the normalized equivalent circuit admittance of the diode elements, formulated previously.

The simplest case, which occurs when operating frequencies are far below the equivalent circuit cutoff frequency, is the array of pure shunt resistances with resistance equal to the Z_0 of the line. This case is plotted in Fig. 4 as the SWR corresponding to $|\Gamma_i|$ and the db loss per element calculated from $|1/T_i|$. Over an octave band the attenuation per diode is quite flat, with a maximum value of 4.2 db and a variation of 0.1 db. Reflection coefficient is quite high for all diodes biased to 50 ohms. However, considerable improvement can be made by tapering into the array with higher impedance end elements. With two end elements having resistances of 2.82 Z_0 and 4.5 Z_0 the reflection is zero at $\theta=60°$ and 120°, and a good match can be maintained over a 4 to 1 frequency band. This is also shown in Fig. 4. Of course, the post geometry for each end element has to be adjusted to give the appropriate impedance and so also does the bias current.

When the operating frequency approaches about one quarter of the equivalent circuit cutoff frequency, the effects of reactance have to be taken into account. Fig. 5 shows plots of the loss per diode as a function of frequency for three values of the resistance when the midband frequency is one quarter of cutoff. The curve for $R=Z_0$ is not much different from the purely resistive case. However, for R larger, the curve rises with frequency, and for R smaller, drops more with frequency. In Fig. 6 the corresponding SWR curves are plotted for the same three values of diode resistance. When end elements of higher impedance are used the SWR can be improved. Fig. 7 shows the results of a computation made for the case of a single end element of twice the impedance of the other diodes in the array. Note that both reactive elements as well as the resistance are doubled. This simply means that the diode post impedance is adjusted to give a circuit impedance Z_c twice

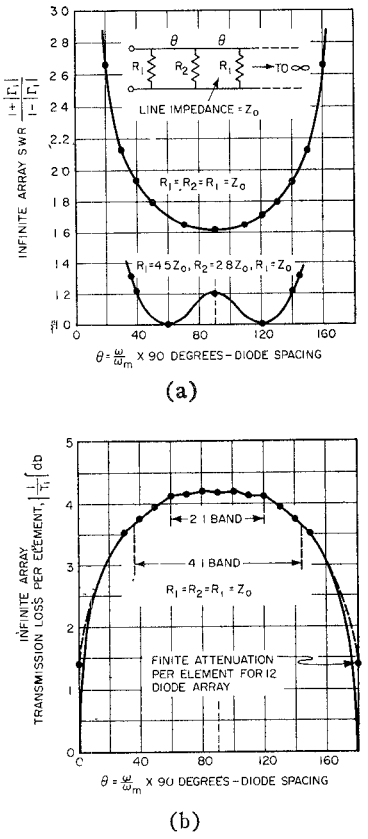


Fig. 4—(a) Theoretical SWR for an infinite array of resistances shunting a transmission line and spaced θ degrees apart. (b) Theoretical transmission loss per element in an infinite array of resistances shunting a transmission line and spaced θ degrees apart.

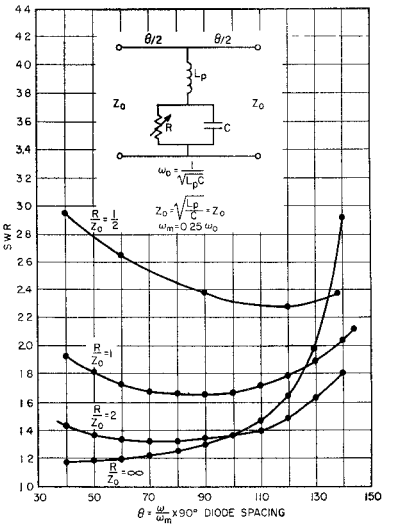


Fig. 6—Theoretical SWR for an infinite array of networks shunting a transmission line and spaced θ degrees apart. Midband frequency, where $\theta = 90°$, is one quarter of the network cutoff frequency.

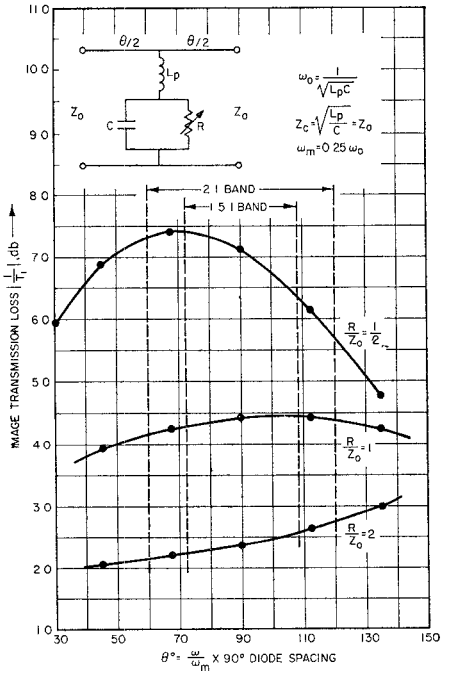


Fig. 5—Theoretical transmission loss per element in an infinite array of networks shunting a transmission line and spaced θ degrees apart. Midband frequency, where $\theta = 90°$, is one quarter of the network cutoff frequency.

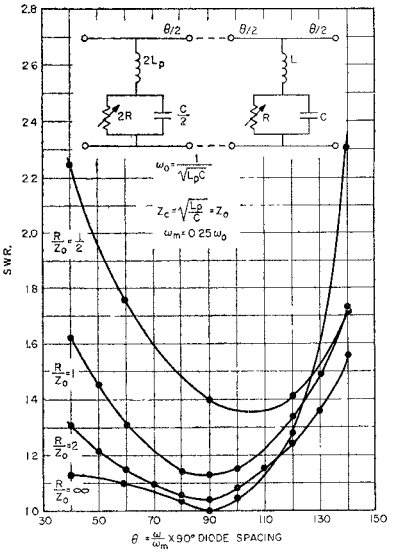


Fig. 7—Theoretical SWR for an infinite array of networks shunting a transmission line and spaced θ degrees apart. The impedance of the first network is twice that of the rest of the networks in the array. Midband frequency, where $\theta = 90°$, is one quarter of the network cutoff frequency.

that of the main line while the bias current is adjusted for a *PIN* junction resistance of twice that of the other diodes. Note that the SWR is improved considerably.

When the diode bias currents are zero, and the attenuation is practically zero, a different method of analysis is applicable. The array is now a capacitively loaded line whose characteristic impedance can be computed from the image parameters of a single capacitance loaded section. It is

$$Z_I = Z_0 \left\{ \frac{1 - \omega^2/\omega_0^2 - (\omega/2\omega_0)(Z_0/Z_c) \tan \theta/2}{1 - \omega^2/\omega_0^2 + (\omega/2\omega_0)(Z_0/Z_c) \cot \theta/2} \right\}^{1/2},$$

where

Z_c = the equivalent circuit impedance,
Z_0 = the unloaded line impedance,
θ = the angular diode spacing ($\theta = \omega/\omega_m \cdot \pi/2$, where ω_m is the midband radian frequency),
ω_0 = the diode equivalent circuit cutoff radian frequency.

The loaded characteristic impedance is frequency dependent and is smaller than Z_0. With the loaded line terminated in Z_0, the input reflection coefficient at any given frequency will be dependent upon the effective loaded line length, and will be a maximum when this length is an odd number of quarter wavelengths. Since attenuators consist of many diodes, this condition will be satisfied at many frequencies within the operating band, so it is instructive to calculate the case of worst reflection as a function of frequency. Assuming the line of impedance Z_I an odd number of quarter wavelengths long and terminated in Z_0, the maximum SWR is $(Z_0/Z_I)^2$. This is plotted in Fig. 6 (labeled $R/Z_0 = \infty$) as a function of $\theta = \omega/\omega_m \cdot \pi/2$, for the case where the midband frequency ω_m is one quarter of the diode equivalent circuit cutoff frequency, ω_0, and may be compared with the SWR curves for the attenuating cases. As expected the SWR increases with frequency. At the upper end of an octave band ($\theta = 120°$) the SWR can be as high as 1.64. This case where $\omega_m = 0.25\omega_0$ is considered to be the practical limit in designing attenuators. Actually, the true SWR oscillates between zero and the infinite R/Z_0 curve.

Improvement in the match can be accomplished by using end elements of lower capacitance. Calculation shows that the capacitance of the end element should be just half that of the elements in the main array for the best match at midband, which means a diode circuit of twice the impedance of those in the array. This case is plotted in Fig. 7 (labeled $R/Z_0 = \infty$) and shows considerable improvement in match over an octave band.

Another important consideration in attenuator design is the zero-bias insertion loss. Since the transmission line is loaded by lossy capacitances at zero bias, the insertion loss is greater than the loss of the line alone. The loss near band center is of the order of

$$\left[A + 8.686n \frac{gZ_0}{2} \right] \text{db},$$

where

A = the db attenuation with no diode loading,
gZ_0 = the normalized zero-bias diode conductance,
n = the number of diodes in the attenuator array.

The capacitive susceptance loading has a negligible effect on the midband insertion loss. The resistive loading can be quite important, as will be demonstrated later with experimental data. Typical values of gZ_0 are of the order of 0.01.

IV. Experimental Results

Before discussing the results obtained with experimental attenuators, it is important to consider some of the practical problems associated with forming an array of diode elements. The biggest problem is the random *PIN* junction characteristics in a given production batch. The effective lifetime varies considerably and the *I* layer thickness may not be perfectly uniform. Some data is shown in Fig. 8 which indicates the effect of these characteristics. The bias current required to produce 50 ohms resistance at 4 Gc was measured for a number of junctions mounted on posts in the strip-line shown in Fig. 1. The effective lifetime of these junctions was then measured by a technique which involved a measurement of the time required for a reverse current to sweep out the stored charge after a very fast change of bias from a known forward current to a known reverse current. Such a measurement yields a time which is really a combination of lifetime and transit-time effects. Junctions with two different *I* layer thicknesses, one twice the other, were used. Not only does the current required to produce a given resistance vary from one diode to another, but so also does the voltage-current relationship. To produce an equal element attenuator whose characteristics can be compared directly with the theoretical characteristics developed in the previous section is difficult unless each individual diode current is controlled. Instead, diodes are usually classified according to the voltage required to produce 50-ohm resistance value and arrays are actually tapered by putting the lower voltage (long lifetime) diodes in the middle and the higher voltage (shorter lifetime) diodes at the ends. All diodes are connected in parallel to receive the same voltage from the bias source, so that a tapering of resistance values occurs.

An 11-diode attenuator was constructed in the unsymmetrical strip-line structure originally described in Fig. 1 with quarter wave length diode spacing at 1.5 Gc. The attenuation as a function of frequency at different bias currents is plotted in Fig. 9(a). The experimental data does not agree too well with the theoretical curves

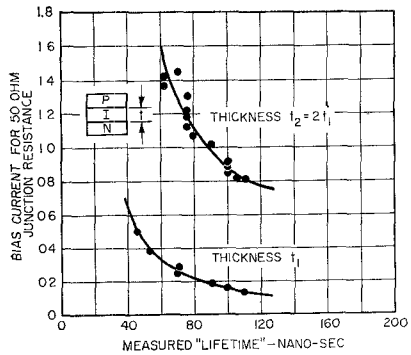
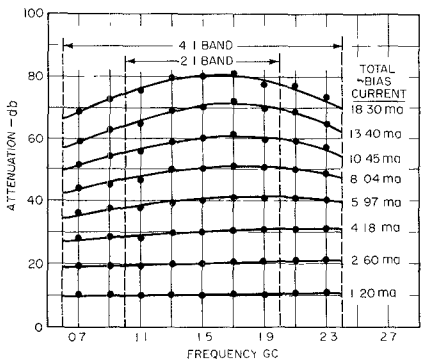
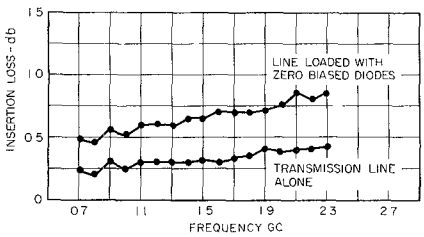


Fig. 8—Experimental data showing the relationship between bias current and lifetime in *PIN* junctions with different *I* layer thicknesses when the microwave resistance is maintained constant at 50 ohms.



(a)



(b)

Fig. 9—(a) Experimental data showing attenuation as a function of frequency at different bias current levels for an 11-diode attenuator array in unsymmetrical strip-line with quarter wavelength diode spacing at 1.5 Gc. Cross-section structure is shown in Fig. 1. (b) Insertion loss of the 11-diode attenuator with and without diodes inserted.

of Fig. 5 for the reasons discussed above and because the diode equivalent circuit cutoff frequencies and impedances are not quite the same for the two cases. The continuous tapering of the diode resistance values in the array is also a factor. The zero-bias insertion loss of the attenuator and the insertion loss of the transmission line alone are shown in Fig. 9(b). The line losses and the diode loading contribute about equally to the total insertion loss. Measured values of diode resistance at zero bias were in the range of 5000 ohms. Using the approximate relation for midband insertion loss given previously, with $A = 0.3$ db, $n = 11$, and $gZ_0 = 0.01$, the loss contributed by diode loading would bring the total insertion loss to 0.78 db which is the order of magnitude observed at midband.

An attempt was made to select diode elements to form an approximately "equal" element array, for which SWR data is presented in Fig. 10(a). Midband SWR values are not far from theoretical values, but variation with frequency is somewhat different. The SWR at zero bias is due chiefly to the reflections from the connectors on the attenuator, which are type *N* with transitions to the strip-line, and the diode loading effect is almost negligible. The SWR of the tapered array for which the attenuation curves of Fig. 9(a) apply, is shown in Fig. 10(b) and indicates the considerable improvement which results from tapering resistance values.

Data is presented in Figs. 11 and 12 on a ridged waveguide attenuator of the type represented in Fig. 3 and Table III. The array consists of 12 diodes spaced a quarter wavelength apart at 10 Gc. The attenuation and SWR curves roughly follow theory when compared to Figs. 5 and 6. Midband frequency is about one quarter of cutoff, although the circuit impedance is low. Attenuation curves tend to rise with frequency at low attenuation levels and tend to drop with frequency at high attenuation levels. The improvement in SWR attained in Fig. 12(b) is a result of tapering the resistance values in the array as discussed before. The diode mounting posts were identical for all elements. The zero-bias SWR shown in Fig. 12(c) is chiefly due to diode capacitance loading, since measurements were made in standard *X*-band waveguide with long tapers connecting to the attenuator and residual SWR was of the order of 1.05. No attempt was made to improve the zero-bias SWR by using higher impedance end-element mounting posts. However, some tapering in diode junction capacitance values may be present.

The manner in which the attenuation of a *PIN* diode attenuator varies with the total applied bias current and applied diode voltage at different temperatures is shown by the experimental data in Fig. 13 over a limited range. This data was taken on a 12-diode attenuator designed for the 2-to-4-Gc frequency band in unsymmetrical strip line and the same voltage was applied to all diodes. The attenuation in db varies almost linearly with current, while the variation with voltage follows the exponential diode law. If a constant diode voltage is maintained, the attenuation rises rapidly with increasing temperature. With a constant current, the attenuation drops with increasing temperature and only by a small amount. The fact that the attenuation varies oppositely with temperature for constant-voltage and constant-current operation suggests that an optimum voltage and source resistance would give temperature compensation. This compensation, however, is only achievable for some particular attenuation level. More sophisticated methods of temperature compensation are possible but have not been tried.

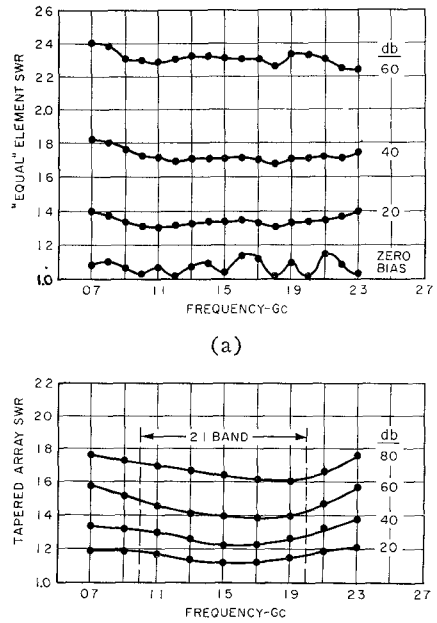


Fig. 10—(a) Experimental data showing the SWR as a function of frequency at different attenuation levels for the 11-diode unsymmetrical strip-line attenuator array with "equal" elements. Diodes are spaced a quarter wavelength apart at 1.5 Gc. Cross-section structure is shown in Fig. 1. (b) SWR of the 11-diode attenuator array with diode positions chosen so that a tapering of junction resistance values occurs at the ends of the array.

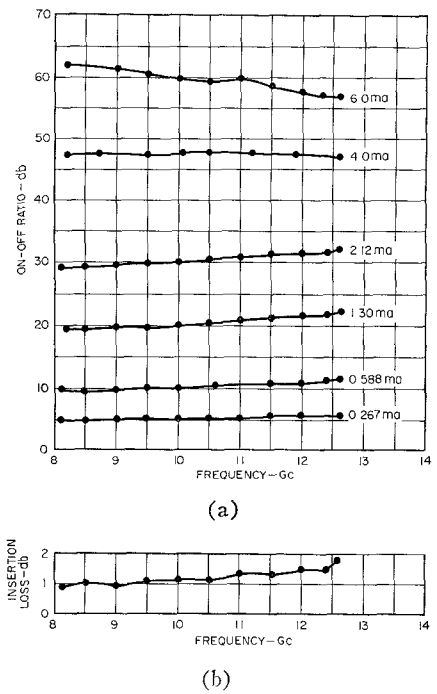


Fig. 11—(a) Experimental data showing the attenuation as a function of frequency at different bias current levels for a 12-diode ridged waveguide attenuator array. Diodes are spaced a quarter wavelength apart at 10 Gc. Cross-section structure is shown in Fig. 3. (b) Insertion loss as a function of frequency for the 12-diode ridged waveguide attenuator with diodes at zero bias.

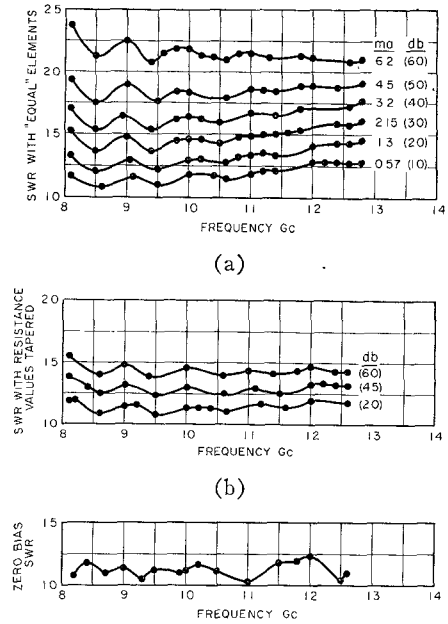


Fig. 12—(a) Experimental data showing the SWR as a function of frequency at different bias current levels for a 12-diode ridged waveguide attenuator array with "equal" elements. Diodes are spaced a quarter wavelength apart at 10 Gc. Cross-section structure is shown in Fig. 3. (b) SWR of the 12-diode ridged waveguide attenuator array with diode positions chosen so that a tapering of junction resistance values occurs at the ends of the array. (c) SWR of the 12-diode ridged waveguide attenuator array at zero bias.

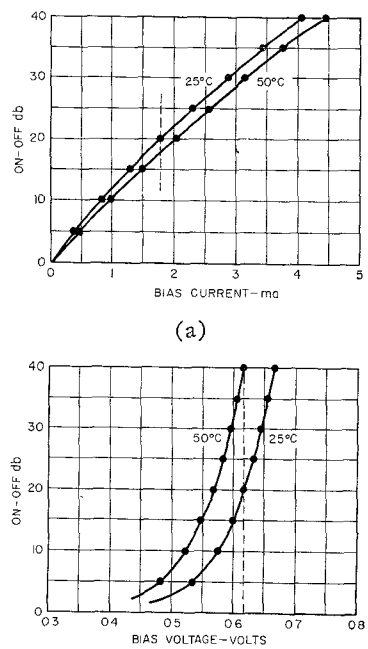


Fig. 13—Experimental data showing the variation of attenuation with bias current and bias voltage at two different ambient temperatures. A 12-diode unsymmetrical strip-line attenuator with a quarter wavelength spacing at 3 Gc was used.

V. High Power Effects

One of the most important effects occurring at high power levels is that of harmonic generation, which can be a serious problem when using diode attenuators over broad frequency ranges. As mentioned earlier, the *PIN* diodes should contribute very little harmonic generation and this is borne out by the experimental curves shown in Fig. 14. The 12-diode strip-line attenuator designed with 3-Gc center frequency was again used for these measurements which were made at 3 Gc. Total harmonic content in the signal output of the attenuator is more than 45 db below the fundamental output at a 1-watt incident power level.

The ultimate power limit of *PIN* attenuators is determined by junction breakdown at high temperature. Some tests were made with a single diode element mounted in the unsymmetrical strip-line structure of Fig. 1. Bias current was adjusted to produce 3-db transmission loss as incident microwave power was gradually increased. Burnout occurred at an absorbed microwave power in the diode of 3 watts, at which time the diode became permanently short-circuited. Examination of the strip-line showed some softening of the plastic dielectric just beneath the center conductor strip at the diode contact point indicating that the junction temperature had reached a few hundred degrees Fahrenheit. Some tests were also conducted on an attenuator array in which the junction resistance values were tapered. The attenuator used for these tests was the ridged waveguide structure described earlier and represented in Fig. 3. Operating frequency was 10 Gc. With diodes biased in parallel with the same applied voltage, a thermal runaway effect and burnout occurred in the first diode of the array at incident power levels approaching 1 watt since, with increasing temperature, the first diode kept absorbing a greater proportion of the incident power. The effect was prevented by placing a resistance of several thousand ohms in series with each individual diode of the array so that each diode received its bias from a constant-current rather than a constant-voltage source. Curves were then plotted of attenuation vs total bias current at different incident microwave power levels. The attenuation range covered was zero to 50 db. Up to an incident power level of 5 watts, the attenuator behaved normally. When the power level was increased to 10 watts, burnout occurred in the third diode of the array as soon as bias current was applied.

From the tests described above, it can be concluded that power levels of the order of 5 watts can be handled by *PIN* attenuatiors provided proper attention is paid to tapering of the junction resistance values in the array, to the maintenance of good thermal contact of the junctions to the transmission line, and to the biasing method providing constant current sources for individual diodes.

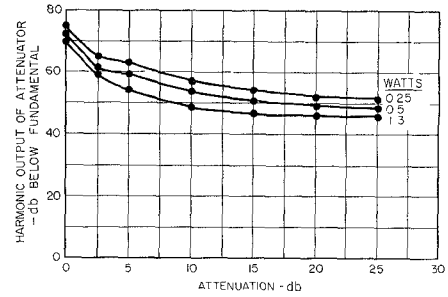


Fig. 14—Experimental data showing the harmonic output level of a 12-diode unsymmetrical strip-line attenuator at different input power levels as a function of the attenuation setting. Diodes in the array are spaced a quarter wavelength apart at 3 Gc. Operating frequency is 3 Gc.

VI. Pulse Modulation

As stated earlier, fast pulse modulation of RF signals is difficult with *PIN* diode attenuators because the stored charge takes some time to build up and decay. With the diodes normally biased with the current required to produce the appropriate "RF OFF" attenuation, it is necessary to remove the stored charge to produce the "RF ON" condition and then restore the charge to produce the "RF OFF" condition again, resulting in a short "RF ON" pulse. If the bias current is merely switched from the normal attenuation value to zero and back again the RF pulse time constant will be very long. Charge build-up throughout the *I* region is a complicated function of diffusion as well as recombination effects. One cannot assume uniform charge distribution in order to get a simple analysis. If it were possible to apply a large quantity of charge to the diode with a current impulse, diffusion would be the governing mechanism initially. If this charge quantity is much larger than that required to produce the steady-state conductivity, the RF pulse would be speeded up in proportion. In an analysis of this nature, an important deduction is that the speed of the diode is limited by the *I* layer thickness and, in fact, varies inversely as the square of this thickness. Thinner *I* layer diodes are to be preferred. However, one has to pay the price of higher attenuator insertion loss because of the lower zero-bias resistance.

To approximate the charge source condition, a large differentiated voltage pulse is applied to the diodes superimposed on the small forward bias required for steady-state attenuation. A pulse modulation experiment was conducted using the 11-diode array for which data was presented in Figs. 9 and 10. Steady-state attenuation was set at 60 db. Rise and decay times of the order of 10 to 20 nsec were achieved with a 15-volt driving pulse. In comparing this device with faster single diode switches, an additional limiting factor is the capacitance of the relatively long length of transmission line which must be charged by the voltage source.

Pulse modulation tests were also made on the 12-diode ridged waveguide attenuator at 10 Gc. In this case, 5000-ohm resistors were placed in series with each diode, each resistor being pybassed by a capacitor to allow direct application of the modulation voltage pulse to the diodes. As discussed previously, the series resistors prevent the thermal runaway effect at high incident power levels. The detected microwave output pulse and the reflected signal at the attenuator input were both observed as the incident CW microwave power level was increased. Pulse shape was maintained with about a 15-nsec rise and decay time, and reflection was low up to an incident power of about 2 watts. At this level, the reflection suddenly increased and the output pulse shape became degraded, indicating breakdown in the initial diodes of the attenuator array. Upon reducing the incident power level, conditions returned to normal, indicating no permanent damage to the diodes.

VII. Conclusion

In conclusion, a comparison between *PIN* diode attenuators and attenuators employing other diode types is appropriate. Garver[2] gives a complete theory of diode switches employing point contact and *P-N* varactor-type diodes and a bibliography of earlier work. Several modes of switching operation are described using a diode both as a series and as a shunt element. The low-frequency shunt element mode corresponds roughly to the operation used here with *PIN* diodes, but inductances and capacitances are so large that the frequency range is quite low. Other modes of operation at higher frequencies involve resonant conditions to obtain attenuation by reflection of the incident power. Multi-element attenuator design would involve reactive filter techniques and bandwidths would be limited. It should be pointed out that high speed switching of microwave power is the goal in Garver[2] and switching speeds of 1 nsec are achieved with the fast diodes which are used. Bandwidths are limited in the case of the point contact diodes because of the high catwhisker inductance and cartridge capacitance, and in the case of the *P-N* varactor diodes, because of high cartridge capacitance and high forward-bias capacitance. When used as a continuously variable attenuator, it would seem that harmonics would be generated, although no data is available.

The shunt capacitance of the *PIN* diode remains low with forward bias. An additional advantage for attenuator design is the broad-band mounting structure with very high cutoff frequency which allows variable resistance operation. Since no encapsulation is used, the attenuator box itself must be sealed against humidity, or the junctions must be sealed by some coating technique.

Attenuators of the type described here are very useful as amplitude levelers for signal generators. In such an application the attenuator is followed by a directional coupler and detector sampling the transmitted signal. Detector output is then amplified and fed back to the attenuator. In addition to maintaining a constant output level, this also results in a very good source impedance match which is very important in many applications. As a pulse modulator the device is capable of a 10-nsec rise time, which is quite good for many applications. The fact that it is well matched in both ON and OFF conditions reduces its frequency pulling effect on the signal source to a negligible amount. Any desired ON-OFF ratio can be achieved by appropriate choice of the number of diodes in the attenuator, and insertion loss is quite low. Powers of the order of watts can be handled with negligible harmonic generation. Octave bandwidths are easily realizable with 4-to-5-db loss per diode. By increasing the number of diodes and operating with lower loss per diode, the flatness of the attenuation characteristic as a function of frequency can, of course, be improved at the expense of insertion loss. The ultimate frequency limit of *PIN* diode attenuators will be imposed by the diode junction shunt capacitance and the finite mounting post length. If the gap in the ridged waveguide structure of Fig. 3 were reduced to 0.015 inch and diodes with 0.035-pf shunt capacitance were used, a cutoff frequency of 61 Gc would be computed. In this case the maximum operating frequency would be of the order of 20 Gc.

Appendix I

Derivation of the Image Parameters for Attenuating Elements

When the attenuator section of Fig. 15 is repeated as an infinite array, the reflection coefficient at the input and output of the section is Γ_i, termed the image reflection coefficient. The flowgraph corresponding to this situation is also shown in Fig. 15. Here Γ, the reflection coefficient of the shunt admittance, Y, when terminated by a matched load, is

$$\Gamma = \frac{-Y/Y_0}{Y/Y_0 + 2}.$$

By the rule for solution of flowgraphs,[3]

$$\Gamma_i = \frac{\Gamma e^{-j\theta}(1 - \Gamma\Gamma_i e^{-j\theta}) + (1 + \Gamma)^2\Gamma_i e^{-2j\theta}}{1 - \Gamma\Gamma_i e^{-j\theta}}$$

which, replacing exponentials by sine and cosine and simplifying, becomes

$$\Gamma_i^2 + 2\Gamma_i\left[\cos\theta - j\sin\theta\left(\frac{1+\Gamma}{\Gamma}\right)\right] + 1 = 0.$$

[3] J. K. Hunton, "Analysis of microwave measurement techniques by means of signal flow graphs," IRE Trans. on Microwave Theory and Techniques, vol. MTT-8, pp. 206–212; March, 1960.

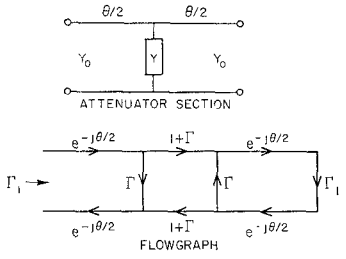


Fig. 15—Attenuator section and flowgraph used for determining image parameters for an array of networks spaced θ degrees apart on a transmission line of characteristic admittance Y_0.

Noting that

$$\frac{1+\Gamma}{\Gamma} = -\frac{2Y_0}{Y}$$

and solving the quadratic equation,

$$\Gamma_i = -\cos\theta - 2j\frac{Y_0}{Y}\sin\theta + \left[-\sin^2\theta\left(1+4\frac{Y_0^2}{Y^2}\right)+2j\frac{Y_0}{Y}\sin 2\theta\right]^{1/2}.$$

The transmission coefficient T_i per element in the infinite array can also be obtained directly from the flowgraph:

$$T_i = \frac{(1+\Gamma)e^{-j\theta}}{1-\Gamma\Gamma_i e^{-j\theta}},$$

and the voltage ratio loss per element is

$$\frac{1}{T_i} = \frac{e^{j\theta}-\Gamma\Gamma_i}{1+\Gamma} = e^{j\theta}\left(1+\frac{Y}{2Y_0}\right)+\frac{Y}{2Y_0}\Gamma_i.$$

Substituting for $e^{j\theta}$ and for Γ_i,

$$\frac{1}{T_i} = \cos\theta + j\frac{Y}{2Y_0}\sin\theta + \left[-\sin^2\theta\left(1+\frac{Y^2}{4Y_0^2}\right)+j\frac{Y}{2Y_0}\sin 2\theta\right]^{1/2}.$$

Appendix II

Derivation of the Image Impedance of Capacitance Loaded Line

Referring to the circuit of Fig. 5 and using the definitions

$$Z_c = \sqrt{\frac{L_p}{C}} \quad \text{and} \quad \omega_0 = \frac{1}{\sqrt{L_pC}},$$

the normalized shunt susceptance at zero bias, or $R=\infty$, is

$$\frac{Y}{Y_0} = \frac{j\dfrac{\omega}{\omega_0}\cdot\dfrac{Z_0}{Z_c}}{1-\dfrac{\omega^2}{\omega_0^2}}.$$

Writing the open- and short-circuit admittances for a half section

$$\frac{Y_{0c}}{Y_0} = \frac{\dfrac{\frac{1}{2}j(\omega/\omega_0)Z_0/Z_c}{1-\omega^2/\omega_0^2}+j\tan\theta/2}{1-\dfrac{\frac{1}{2}(\omega/\omega_0)(Z_0/Z_c)}{1-\omega^2/\omega_0^2}\tan\theta/2}$$

$$\frac{Y_{sc}}{Y_0} = -j\cot\theta/2.$$

The normalized image impedance is then,

$$\frac{Z_I}{Z_0} = \left(\frac{Y_0^2}{Y_{0c}Y_{sc}}\right)^{1/2} = \left\{\frac{1-\dfrac{\omega^2}{\omega_0^2}-\dfrac{\omega}{\omega_0}\cdot\dfrac{Z_0}{Z_c}\tan\dfrac{\theta}{2}}{1-\dfrac{\omega^2}{\omega_0^2}+\dfrac{\omega}{\omega_0}\cdot\dfrac{Z_0}{Z_c}\cot\dfrac{\theta}{2}}\right\}^{1/2}.$$

Acknowledgment

The authors wish to express their thanks to H. E. Overacker, L. Madden, and H. E. Hiner for their contributions in the manufacturing of *PIN* junctions suitable for microwave attenuators, and also to J. L. Moll, J. G. Linvill, and R. B. Riley for their contributions to the proper understanding of the semiconductor physics.